AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to FIGS. 1, 2, and 3 labeling FIG. 1, FIG. 2, and FIG. 3 as --BACKGROUND ART-- as described in the pages 1-6 of the Specification. Additionally, reference characters "$Lout_{(Inv)}$" and "$Lout_{(Non\text{-}inv)}$" have been added to distinguish the inverted and non-inverted Lout as shown in FIGS. 2, 3, 4, and 5, as described in page 5, line 21 – page 6, line 17 and page 11, line 24 – page 12, line 11. Also, "VSS~HVSS2" has been deleted from FIG. 4. *These amendments include no new matter.*

Attachment: Replacement sheet
Annotated sheet showing changes

REMARKS

This amendment is responsive to the Office Action dated October 20, 2008. Claim 1 is currently amended. New claim 3 has been added. Support for these amendments may be found variously throughout the Specification, for example on page 9, lines 26 – page 12, line 13. *These amendments add no new matter.* In the amendment, claim 1 remain pending in the application. Reconsideration and allowance of the pending claims are respectfully requested.

Objections to the Drawings and Specification

The attached sheets of drawings include changes to FIGS. 1, 2, and 3 labeling FIG. 1, FIG. 2, and FIG. 3 as --BACKROUND ART-- as described in the pages 1-6 of the Specification. Additionally, reference characters "$Lout_{(Inv)}$" and "$Lout_{(Non\text{-}inv)}$" have been added to distinguish the inverted and non-inverted Lout as shown in FIGS. 2, 3, 4, and 5, as described in page 5, line 21 – page 6, line 17 and page 11, line 24 – page 12, line 11. Also, "VSS~HVSS2" has been deleted from FIG. 4. *These amendments add no new matter.*

Additionally, as per the Examiner's request, and in accordance with 37 C.F.R. 125, the Specification has been amended to bring the drawings into conformity with 37 C.F.R. 1.83 and 1.84. Specifically, page 5, line 27 has been amended to correct a typographical error by deleting "(FIG. 9(E))" and inserting --(FIG. 3(E))-- in its place, and at page 6, lines 9 and 12, respectively, reference characters OE1 and 2Lout have been properly added to the Specification. *These amendments add no new matter.*

Claim 1 has been rejected under 35 U.S.C. § 112, ¶2, as being indefinite for failing to particularly point out and distinctly claim what Applicant regards as the invention.

Applicant appreciates the Examiner's attention to claim 1 in this regard, and has amended claim 1 to clarify essential structural cooperative relationships.

Applicant submits that claim 1 now particularly points out and distinctly claims the subject matter which Applicant regards as his invention. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1 as being indefinite under 35 U.S.C. § 112, ¶2.

Claim 1 has been rejected under 35 U.S.C. § 102(a) as being anticipated by what is referred to in the Office Action as Application's Admitted Prior Art (AAPA). This rejection is respectfully traversed.

For a *prima facie* case of anticipation, each and every element set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Furthermore, to be anticipated, the identical invention must be shown in as complete detail as is contained in the patent claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1, as amended, recites: *[a] data transfer circuit for latching an input data in a first latch section, transferring a first latch result of said first latch section to a second latch section, and latching said first latch result in said second latch section, characterized by:*

transferring only an inverted output of said first latch result to said second latch section or transferring only a non-inverted output of said first latch result to said second latch section; and

raising a power supply voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section;

wherein said second voltage is higher than said first voltage and,

wherein said second voltage is a power supply voltage of said second latching section.

AAPA does not disclose or suggest these claimed features. Specifically, AAPA fails to disclose or suggest "*transferring **only** an inverted output of said first latch result to said second latch section **or** transferring **only** a non-inverted output of said first latch result to said second latch section*[.]"

It should be noted that, as disclosed by AAPA, "an inverted output $1Lout_{(Inv)}$ of a latch result by this first latch section 21 ***and*** a non-inverted output $1Lout_{(Non\text{-}inv)}$ thereof are inputted to the second latch section 22[.]" (Clean Substitute Spec., page 5, lines 21-28 (emphasis added).)

The Office Action infers that it would be possible for either the transfer switch 25 or the transfer switch 24 to "never" output an inverted or non-inverted output. (Office Action, pg. 13, lines 20-23.) However, AAPA clearly discloses that both transfer switches 25, 24 turn to an ON-state at a timing OE1. As shown in FIG. 2, timing OE1 turns transfer switches 24, 25 "ON-state". (Clean Substitute Spec., page 5, lines 25-27.) AAPA does not suggest that timing OE1 selectively turns one switch to an ON-state while the other transfer switch "never outputs" an output, either inverted or non-inverted.

Accordingly, AAPA fails to disclose or suggest "*transferring **only** an inverted output of said first latch result to said second latch section **or** transferring **only** a non-inverted output of said first latch result to said second latch section*[.]"

Additionally, while FIG. 3(C) and 3(D) disclose the inverted and non-inverted output voltages $1Lout_{(Inv)}$ and $1Lout_{(Non\text{-}inv)}$ rising and falling with timing SP, AAPA clearly fails to disclose or suggest "*raising a power **supply** voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section*[.]"

Because AAPA clearly fails to disclose or suggest each and every element set forth in claim 1, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 as being anticipated by AAPA under 35 U.S.C. § 102(a).

Claim 1 has been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pub. No. 2003/0011584 A1 to Azami et al. ("Azami").

Again, for a *prima facie* case of anticipation, each and every element set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Furthermore, to be anticipated, the identical invention must be shown in as complete detail as is contained in the patent claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Like AAPA, Azami fails to disclose each and every element set forth in claim 1. Specifically, However, Azami clearly fails to disclose or suggest "*raising a power supply*

voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section;

wherein said second voltage is higher than said first voltage and,

wherein said second voltage is a power supply voltage of said second latching section."

Azami discloses first latch circuit and the second latch circuit used in the light emitting device wherein "a digital image signal is input (data in) from an input electrode of a TFT 1850, and a sampling pulse is input (pulse in) to a gate electrode, turning the TFT 1850 on, then the digital image signal is input to an inverter composed of TFTs 1851 to 1854 and a capacitor 1855, the polarity is inverted[,]" and "the digital image signal is also written into, and stored in, the second latch circuit by similar operations in accordance with a latch pulse (LAT) input timing." (Azami, para. [0183]-[0186].)

However, Azami clearly fails to disclose or suggest "*raising a power supply voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section;*

wherein said second voltage is higher than said first voltage and,

wherein said second voltage is a power supply voltage of said second latching section."

Because Azami fails to disclose or suggest each and every element set forth in claim 1, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 as being anticipated by Azami under 35 U.S.C. § 102(b).

Alternatively, claim 1 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pub. No. 2003/0011584 A1 to Azami et al. ("Azami") in view of Japanese Pat. No. 2000-221926 A to Nakajima et al. ("Nakajima"). This rejection is respectfully traversed.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); *see also* MPEP 2143.03.

As described above, Azami clearly fails to disclose or suggest "*raising a power supply voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section;*

wherein said second voltage is higher than said first voltage and,

wherein said second voltage is a power supply voltage of said second latching section."

Nakajima fails to remedy the deficiencies of Azami. Nakajima discloses a CMOS latch cell 30 having CMOS inverters 31, 32. (Nakajima, para. [0037]-[0038], Drawing 5.) Nakajima discloses that "in the period of latch operation with active output enable pulse eo1, it operates under VDD1 power supply[.]" (Nakajima, para. [0043].) Further, Nakajima discloses that in the period of active output operation, "the power supply by the side of right of CMOW latch cell switches from VDD1 power supply to VDD2 power supply[,]" and that "power-supply-voltage VDD2 [is] higher than power-supply-voltage VDD1." (Nakajima, paras. [0044] and [0040].)

However, Nakajima fails to disclose "*raising a power supply voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section...*

wherein said second voltage is a power supply voltage of said second latching section."

This feature is significant as Applicant's invention is intended to propose a simplified construction of a data transfer circuit. (Clean Substitute Spec., page 6, lines 18-27; page 15, line 31 – page 16, line 10.)

Accordingly, because Azami and Nakajima, either alone or in any permissible combination, fail to teach or suggest each and every feature of claim 1, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Azami in view of Nakajima.

CONCLUSION

In view of the foregoing arguments, all claims are believed to be in condition for allowance. If any further issues remain, the Examiner is invited to telephone the undersigned to resolve them.

This response is believed to be a complete response to the Office Action. However, Applicant reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly do not acquiesce to the taking of Official Notice, and respectfully request that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 C.F.R. § 1.104(d)(2) and MPEP § 2144.03.

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Respectfully submitted,

By _____

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